REMARKS

Reconsideration of this application, in view of the foregoing amendments and the following remarks, is respectfully requested.

Drawings

Figure 1 has been objected to for not containing the legend "Prior Art". Applicants have resubmitted the replacement sheet with correct legend for figure 1.

Claim Rejections - 35 USC § 102

Claims 5-7 are rejected under 35 U.S.C. 102(e) as being anticipated by New (U.S. Patent 5,956,748). Applicants respectfully traverse these rejections.

To anticipate a claim under 102(e), the reference must teach every element of the claim. *See* MPEP §2131. As to claim 5, New does not teach each and every element of the claim.

Regarding claim 5, the Examiner has stated that New discloses:

> responsive to a write valid bit **associated with** a first one of the plurality of entries indicating that the first one of the plurality of entries does not contain valid data, the first one of the plurality of entries indicated by a current value of a write pointer: storing the applied data word into the first one of the plurality of entries (figure 2, elements 203 and 205 as described in col. 4, lines 42-50); (Emphasis added)

Applicants respectfully disagree. In the cited sections, New describes the write function of the memory. The write operation in New is initiated by the write control unit 203 by enabling the write address counter 205. The memory location to be written is identified by the write address counter 205. However, in the cited sections, New does not describe **a write valid bit associated** with a first one of the plurality of entries as recited in claim 5. In fact, the write operation in New is stopped only when the FULL signal is asserted, which basically shuts the entire write operation (*see* col. 6, line 62 – col. 7, line 42). Nowhere in the cited sections New describes a write valid bit associated with memory location indicating the validity of data as

recited in claim 5. The Examiner has further stated that "whereby enabling the write operation the write bit has been set" (emphasis added). Applicants respectfully point to the Examiner that first, New does not even describe a write valid bit associated with buffer entries; second, as explained above, the write operation is initiated by the write control unit according to the FULL flag. Once the FULL flag is asserted low, the write operation continues regardless of the content of the corresponding memory location. Accordingly, New does not disclose write bit associated with buffer entries as recited in claim 5.

Further as to the read bit, the Examiner has stated that "whereby enabling the read operation **the read bit** has been set" (emphasis added). Applicants respectfully point to the Examiner that New does not even describe a read bit associated with buffer entries. Thus, there is no need for setting the read bit. In the cited sections, New describes read operation, which is controlled by the read control unit 204 according to the EMPTY flag. Just like the write operation, the read operation continues until the EMPTY flag is asserted. The read operation of New does not depend on the validity of data in each entry and as long as the EMPTY flag is not asserted, the read control continues to read the data regardless of its validity. In fact, even New describes that at times, the EMPTY flag may be asserted "unnecessarily", which may prevent read from one or more of the last data values from the memory locations (*see* col. 6, lines 5-18). Similarly, New states that the FULL flag me by asserted "unnecessarily" preventing the dual-port memory from being completely filled (*see* col. 7, lines 29-42). Thus, the read and write operations in New do not depend on any read/write valid bits associated with buffer entries as recited in claim 5. Therefore, New does not describe a read valid bit associated with buffer entries as recited in claim 5.

Similarly, because New does not describe read/write valid bits associated with buffer entries, there is no need in New to clear these bits. Therefore, New does not teach each and every element recited in claim 5 and does not anticipate claim 5. Accordingly, claim 5 is patentably distinguishable from New.

Claims 6-7 depend from claim 5 and are patentably distinguishable from New for at least the same reasons as claim 5.

Claim Rejections - 35 USC §103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over New (U.S. Patent 5,956,748). Applicants respectfully traverse these rejections.

There are three basic criteria to establish a *prima facie* case of obviousness under 35 U.S.C. §103(a). First, there must be some suggestion or motivation in the cited references to modify or combine their teachings; second, there must be reasonable expectation of success; and third, the prior art references must teach or suggest all the claim limitations. *See* M.P.E.P §2142. As to claim 1, New does not teach or suggest all the claim limitations.

As to claim 1, the Examiner has stated that "figure 2, elements 241 and 240 act as valid logic circuits by enabling the read and write operations." Applicants respectfully point to the Examiner that claim 1 recites a plurality of valid logic circuits, **each associated with a corresponding one of the plurality of entries of the buffer**. New does not show valid logic circuits associated with entries of buffer. In fact, elements 241 and 240 are FULL and EMPTY flag generator. According to New, the EMPTY flag is only asserted when the write address SYNC_WA and the current read address CURRENT_RA are equal meaning all locations in the dual-port memory have been read (*see* col. 5, line 25 – col. 7, line 18). The EMPTY flag generator 240 is not associated with corresponding one of the entries in the buffer and does not depend on the validity of the content of associated entry in the buffer as recited in claim 1. The EMPTY flag is monitored by the comparator 208. Similarly, the FULL flag generator is also not associated with each one of the corresponding entries in the buffer instead and does not depend on the validity of the contents of associated entries in the buffer instead, it is monitored by comparator 207 to determine the equality of SYNC_RA and CURRENT_WA signals (*see* col. 6, line62 – col. 7, line 42). Further as explained above, the FULL and EMPTY signals may also be asserted "unnecessarily." Therefore, New does not show, teach, or describe valid logic circuits each associated with a corresponding one of entries in the buffer as recited in claim 1.

Similarly, because New does not describe valid logics associated with corresponding entries in the buffer, New also does not describe any of the structural elements of these valid logic circuits. The Examiner has cited latches of FULL flag generator and EMPTY flag generators; however, as describes above, these generators are not valid logics associated with corresponding entries in the buffer. Therefore, New does not describe read valid latches and write valid latches as recited in claim 1.

As to the reset logic, the Examiner has cited various elements used to reset the FULL and EMPTY flag generators in New; however, as explained above, these generators are not associated with corresponding entries in the buffer, therefore, New does not describe reset logics for resetting write and read valid logics each associated with corresponding one of the plurality of entries of the buffer as recited in claim 1.

Further, the Examiner has stated that:

> "However, New does not explicitly show that "each valid logic circuit" contains the **write latch**, **read latch**, **reset logic**, and **set logic**. Although New shows the valid logic circuits on either side of the figure, it would have been obvious to one with ordinary skill in the art at the time of invention to have all of the components of elements 240 and 241 (i.e. the write latch, read latch, reset logic, and set logic) combined into a single unit as a matter of design choice. The layout and placement of components in a given system are motivated by designer preference and the desired outputs are equivalent." (Emphasis added).

First, even though the Examiner has admitted that New does not explicitly show the write latch, read latch, reset logic, and set logic; however, the Examiner has still cited various elements for example, for write valid latch – element 214, for read valid latch – element 212; for reset logic – elements 207, 221, and 223; and for set logic – elements 208, 222, and 224.

Second, the Examiner has stated that "it would have been obvious to one with ordinary skill in the art at the time of invention to have all of the components of elements 240 and 241 (i.e. the write latch, read latch, reset logic, and set logic) **combined into a single unit** as a matter of design choice." (Emphasis added). Applicants respectfully point to the Examiner that as explained above, New does not describe various logic circuits associated with corresponding entries in the buffer. Further, the elements described by the Examiner as combined into a single

unit as a matter of design choice actually belong to two difference clock domains and provide different functions. Thus, they cannot be combined into a single unit. Accordingly, New does not show, teach, or suggest each and every limitation of claim 1 and claim1 is patentably distinguishable from New.

Claim 2 depends from claim 1 and is patentably distinguishable from New for at least the same reasons as claim 1.

Claims 3 and 4 depend from claim 1 and are patentably distinguishable from New for at least the same reasons as claim 1. Further, as to claims 3 and 4, as explained above, New does not show, teach, or describe read/write valid logics for each one of the corresponding entries in the buffer. Therefore, there is no need to include set/reset logic components as described in claim. Accordingly, claims 3 and 4 are further patentably distinguishable from New.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over New in view of Finney et al. (U.S. Patent 5,487,092). Applicants respectfully traverse these rejections.

First, claim 9 depends from claim 5, which has been distinguished from New for failing to disclose each and every element of claim 5. Therefore, the combination of New and Finney et al. cannot render clam 9 obvious.

Second, as to the motivation of inserting pad words of Finney in the scheme of New, the Examiner has stated that

> "It would have been obvious to one of ordinary skill in the art at the time of invention to include the inserting of the idle symbol for the purpose of providing for the "necessary flow control." The motivation for inserting the idle symbol is to effectively aid in synchronizing data flow between two different frequencies (or clocks). (Emphasis added)

Applicants respectfully point to the Examiner that Finney et al. uses two distinct sets of internal and external registers (28 and 38). Finney et al. adds pad words to the outgoing data to compensate for pad words received in the incoming data as identified by the idle decode unit 26. Further, the pad words are used to compensate for clock oscillator inaccuracies (*see* col. 7, lines 22-25). In contrast, New uses a sync engine 210 to synchronize read and write operations (*see*

col. 7, line 43- col. 9, line 7, figures 2 and 3). Thus, because of the sync engine 210, there is no need to add any pad words or idle symbols in New. In fact, for New, it does not even matter whether a data word is an idle symbol, pad word, or a valid data because it does not rely on the contents of the data word to synchronize the operations. The incoming data in New is received on the write port 232 and is outputted on the read port 231 (*see* figure 2) and the control circuit does not receive the content of the data. Therefore, not only it will not be obvious to include idle symbols in New but in fact, one skilled in art will consider it as a waste of data bandwidth. Accordingly, there is no motivation in New to include pad words of Finney et al. and in fact, New teaches away from using any other means for the synchronization of read and write operations besides the sync engine 210. Therefore, claim 9 is further patentably distinguishable from the combination of New and Finney et al.

Claims 10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lowe et al. (U.S. Patent 6,233,221 131) in view of New. Applicants respectfully traverse these rejections.

The Examiner has not identified elements in the cited references teaching each an every limitation of claim 10. For example, as to the plurality of switches having interfaces and the plurality of switch fabric devices including switch interface, the Examiner has cited switch fabrics 209 and 205 of Lowe et al. and stated that "it is commonly known in the art that **switch fabrics contain a plurality of switches** to operate on a plurality of data inputs." Applicants respectfully point to the Examiner that claim 10 recites two distinct elements: 1) Switches with interfaces, and 2) Switch Fabrics with recited elements coupled to one of the switches. The Examiner has assumed that switches are included in the switch fabrics 205 and 209, which is not supported by the description of Lowe et al.

Further, as to the first receive ring interface operating in a receive clock domain as recited in claim 10, the Examiner has cited element 204. Applicants respectfully point to the Examiner that actually claim 10 recites that the switch fabric comprises the first receive ring interface. In contrast, the ring interface module 204 of Lowe et al. includes the switch fabric 209. Similarly, the Examiner has cited element 202 as the transmit ring interface operating in a transmit clock domain. Applicants respectfully point to the Examiner that in fact, both of these elements, 202 and 204, are part of a single Network Element 'NE', which also includes the switch fabric.

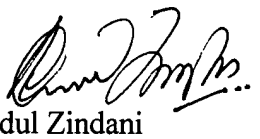
Further, as to the transmit clock generator, the Examiner has cited the clock in New and stated that "if a clock signal exists in the system, it must have been generated by a device." Applicants respectfully point to the Examiner that first, claim 10 recites two distinct clock domains: 1) receive clock domain and 2) transmit clock domain. Second, the elements cited by the Examiner are included in a single unit of Lowe et al. and there is no mention of two different clock domains in Lowe et al. The Examiner has also not cited two different clock domains in Lowe et al. or a need for different clock domains therein. Therefore, the combination of New and Lowe et al. do not teach all limitations of claim 10.

Furthermore, the Examiner has rejected the remaining elements of claim 10 in the manner of claims 1 and 5 in view of New. Therefore, these elements are patentably distinguishable from the combination of New and Lowe for at least the same reasons as claims 1 and 5.

Claim 15 depends from claim 10 and is patentably distinguishable from the combination of cited references for at least the same reasons as claim 10. Further, the Examiner has cited various synchronization elements of New to be included in the system of Lowe et al. Applicants respectfully point to the Examiner that Lowe et al. does not describe two different clock domains as recited in claim 15 and thus, there is no need to include synchronization elements as stated by the Examiner. Furthermore, Lowe et al. discloses a closed-loop ring network (*see* col. 3, lines 46-50), which does not include multiple clock domains as recited in claim 15. Accordingly, claim 15 is further patentably distinguishable from the combination of cited references.

Applicant believes this application and the claims herein to be in a condition for allowance. Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,



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